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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,154	BURGENER ET AL.	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10, 12-20, and 22-67* is/are rejected.

7)☒ Claim(s) *11, and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Feb 13, 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figs. 1-2 should be designated by a legend such as --Prior Art-- because only that which is old is believed to be illustrated. See MPEP § 608.02(g). For example, Fig. 1 is described in the Background of the Invention section, and Fig. 2 is described as "basic charge pump operations", wherein one of ordinary skill in the art would clearly understand both figures with respect to prior art references and/or knowledge. Therefore, corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicants will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The applicants are reminded of the proper language of an abstract. In this case, the phrase "is described" within the first sentence is implied since it is understood that an abstract should be describing the claimed invention in a summarized version. Therefore, it is suggested "is described having" be replaced with --have--. This removes the implied understanding, as well as removing a syntax error (i.e. "charge pump method and apparatus is").

The disclosure is objected to because of the following informalities: Page 8, line 31 "362" should be --364-- because that is the reference designator clearly shown in Fig. 3 as being coupled to the gate of switch 312. Related to this, "364" on line 1 of page 9 should be --362--.

Page 17, lines 9-10 need to be clarified with respect to having Vd 910 connected to Vs+, wherein Vd 910 is driven to –3*Vs+. For example, isn't output Vb 906 driven to the negative boosted voltage? Page 18, line 13 "1017" should be --1016--. Appropriate corrections are required.

Claim Objections

Claims 2 and 10 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. The applicants are required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Since the "plurality of transfer capacitor coupling switches" is already "under the control of a charge pump clock output", how does claim 2 further limit that? Related to this, with the coupling switches of claim 1 controlled by the charge pump clock output (i.e. see lines 3-4) to couple the transfer capacitor to the voltage source (i.e. see line 9), one of ordinary skill in the art would understand that corresponds to claim 10's "coupling the transfer capacitor to the voltage source via the charge pump clock output" (e.g. without the proper clock output, the capacitor will not be coupled to the voltage source).

Claims 12-17, 26-27, 32, 35, 37, 39, 45, 47, 49-59, 62-65, and 67 are objected to because of the following informalities: To minimize possible confusion with respect to "an active driver circuit" in claim 12 (line 5) with "a plurality of active driver circuits" in claim 14 (lines 1-2), it is suggested the line 5 phrase in claim 12 be changed to --at least one active driver circuit--. For similar reasons, it is suggested each occurrence of "each active driver circuit" on lines 4-5 of claim 14 be changed to --each of the active driver circuits-- to more clearly refer back to the plurality of circuits cited on lines 1-2 of claim 14. Claim 26, line 1 ""each capacitive coupling circuit" should be –each of the capacitive coupling circuits—to more clearly relate back to the

first/second circuits of claim 25. Claim 27 "a voltage source" (line 2) is believed to mean --the voltage source-- to refer back to "a voltage source" in claim 24. It is believed "voltage source" on line 1 of claim 32 was meant to be --source voltage-- to relate back to "the "source voltage" recited within claims 28 (e.g. lines 1-2) and 29 (line 2). If "a control node of each actively controlled TCCS circuit" on line 2 of claim 35 relates to the limitations recited on line 1 of the same claim, it is suggested the line 2 phrase be changed to --the control node of each of the actively controlled TCCS circuits--. Claim 37, line 1 should have both occurrences of "current" changed to --currents-- to correspond to the "currents" recited within claim 36. The term "the" should be added prior to both "source" and "sink" on line 1 of claim 39 since those currents were apparently recited previously within claim 36. For consistent labeling throughout the claims, it is suggested --output-- be added prior to "node" on line 1 of claim 45. Claim 49, line 5 "the voltage source" should be --the source voltage-- to relate back to "a source voltage" recited on line 1 of the same claim. Line 1 of both claims 51 and 53 cite "a voltage source", but this is believed to mean --the source voltage-- to clearly refer back to "a source voltage" on line 1 of claim 49. Related to this, it is also believed "a second voltage source" on line 2 of claim 54 should be --a second source voltage--. It is suggested both occurrences of "each actively... switch" on line 2 of claim 55 be changed to --each of the actively...switches-- to more clearly relate back to the first/second TC charging and discharging switches of claim 54. To more clearly relate "a driver circuit" of claim 59, lines 2-3 to "each driver circuit" of claim 58, it is suggested "a driver circuit" in claim 59 be changed to --one of the driver circuits--. Since claim 60 has first/second capacitive coupling networks, it is suggested "each capacitive coupling network" on line 1 of claim 62 be changed to --each of the capacitive coupling networks--.

Claim 67 "all charge" should be --all of the charge-- to clearly refer back to the "corresponding charge pump clock output" recited within claim 66. Dependent claims carry over any objection(s) from any claim(s) upon which they depend. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3-9, 12-27, 31-32, 34-39, 41-42, 46-47, 52, 56, and 60-67 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. It is not clear in claims 3-4 how the current source/sink limit devices relate to the "circuitry" on lines 6-7 of claim 1 which already limit the rise/fall rates. For example, how are the devices of claims 3-4 different from the "circuitry" in claim 1? It is not understood if "a transfer capacitor coupling switch" in claim 5 actually relates to one of the plurality recited within claim 1, or possibly to another type of coupling switch. It is not clear how claim 6's "a common charge pump clock output" relates to the singular "a charge pump clock output" recited on line 4 of claim 1. For example, does the common output of claim 6 imply that the singular clock output of claim 1 can actually comprise more than one clock output signal (e.g. signals with different phases)? Similar to claims 3-4 above, it is not clear how the circuitry to limit currents in each of claims 7-9 relate to the circuitry for limiting rise/fall rates recited within claim 1. For example, if the current is limited, doesn't that in itself limit the rise and/or fall rate? Claim 14, lines 3-4 cite "circuitry" for limiting current, without clarifying how this "circuitry" relates to those current limiting circuits cited in claim 12, lines 8 and 10. It is not clear in claim 15 how the "charge pump clock output signal"

and "an active switch" relate to the "charge pump clock output" and "plurality of active switches" recited within claim 12. The use of "a second charge pump stage" on line 1 of claim 19 implies a first stage that has not been clearly identified. For example, does it refer to the charge pump apparatus of claim 18, or just certain parts of it? Some of the limitations within claim 18 can be considered misleading and/or confusing. For example, it is not clear in claim 18 how "all of the source switching devices" (lines 8 and 9) and "all of the output switching devices" (lines 10 and 11-12) would relate to the switching devices of lines 3 and 5 if there is only one of each. For example, does the use of "all" refer to at least two, or was "all" meant to be --each--? Claim 19, lines 7 and 9 have the same type of problems as claim 18, wherein claim 19 cites "all of the second-source switching devices" and "all of the second-output switching devices." It is not clear how "a charge pump clock generating circuit" in claim 22 relates to "a charge pump clock generating circuit" already recited within claim 18. Claim 23 needs clarification with respect to how its "an amplifying driver circuit output" relates to claim 22's "each amplifying driver circuit". For example, can this output be from some other driver circuit? Clarification is requested with respect to how "a control node", "a source switching", and "an output switching device" on lines 7-8 of claim 24 relate to the "one or more" switching devices, and their "corresponding control node" recited within lines 3-6 of the same claim. Similarly, how do "a charge pump clock output", "a source switching device control node", and "an output switching device control node" of claim 25 relate back to the clock output and control nodes recited within claim 24? Also, how do the first/second capacitive coupling circuits of claim 25 relate back to the "capacitive coupling circuit" of claim 24? Clear relationships between elements within each claim, and within related claims, will minimize confusion. For example,

related to the coupling circuit problems of claim 25, how does "each capacitive coupling circuit" of claim 26 relate to the "capacitive coupling circuit" of claim 24, and to the first/second capacitive coupling circuits of claim 25? Also, is claim 26's "switching device" related to one of the switching devices recited within claims 24 and 25, or to some unknown switching device? If the phrases "all source switching devices" and "all output switching devices" in claim 27 imply more than one of each switching device, how would "all" relate to just one as the "one or more" phrases in claim 24 can provide? It is not clear how "an output voltage" and "a common clock output" of claim 27, line 3 clearly relate to the "output voltage supply" and "charge pump clock output" of claim 24. It is not clear in claim 34 if "a TCCS circuit" relates to the TCCS circuit of claim 28, or if it can be some other circuit. How does the plural "actively controlled TCCS circuits" in claim 35 relate to the single "TC-coupling switch ("TCCS") circuit" of claim 28, line 3, or to "a discharging TCCS circuit" of claim 28, line 5? It is not understood if "a clock generator driver circuit" on line 4 of claim 36 refers back to the first driver circuit recited on line 1 of the same claim, or to some other driver circuit. It is not understood how claim 39 can recite the plural implying phrase "all first clock generator driver circuits" when claim 36 only recites the singular "a first clock generator driver circuit" on line 1. It is not clear how the coupling and "passive TCCS circuit" of claim 41 relates to the coupling and "a discharging TCCS circuit" already recited within claim 28. Similarly, it is not clear how the coupling and "a discharge output TCCS" of claim 42 relate to the coupling and "discharging TCCS circuit" recited within claim 28. The use of "each driver circuit" in line 1 of each of claims 46 and 47 appears to imply more than one. However, claim 43, line 5 cites only "a driver circuit." It is not clear in claim 52 how the "first TC discharging switch device" (lines 2 and 7) relates to the "TC discharging

switches" recited within claim 50, or to the singular "TC discharging switch" in claim 49. For example, are the "switches", the "switch", and the "switch device" all referring to the same "TC discharging" element? The use of "each actively...switch" in line 2 of claim 56 appears to imply more than one of each switch. However, claim 49 only cites the singular "a TC discharging switch" and the singular "a TC charging switch" in lines 3 and 5, respectively. It is not clear if "the switch device" of claim 62 refers only to "the discharging switch device" of claim 60, or to the charging and discharging switches of claim 60. It is not understood if the same TC, or another TC, is coupled to the source voltage by the second TC charging switch as recited within claim 63. For example, where in the figures, or the disclosure, is the same TC coupled to the source voltage by two TC charging switches? For reasons similar to claim 63 above, what figure(s) or page(s)/line(s) show or disclose two discharge switches that couple the TC to the output supply during the discharge periods as recited within claim 65? It is not clear how "each actively controllable TC coupling switch" and the "capacitively coupling" recited within claim 66 relates to the TC charging/discharging switches, and the first/second capacitive coupling networks as recited within claim 60.

Claims 12-17 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are related to how the "driver output node" of claim 12 actually relates to: "output connections" and "charge pump clock output" also recited within the claim (e.g. see lines 2 and 4).

Claim 23 recites the limitation "the driver circuit's voltage output" in line 2 with insufficient antecedent basis for this limitation in the claim. For example, does this refer back to the "amplifying driver circuit output" in claim 23, or some other output?

Claim 31 recites the limitation "the first charge pump output" in lines 1-2 with insufficient antecedent basis for this limitation in the claim. For example, does this refer back to the "output supply from a charge pump" recited on line 1 of claim 28? If it does, how does this output actually control all the TCCS circuits?

Claim 60 recites the limitation "the discharging switch device" in line 9. There is insufficient antecedent basis for this limitation in the claim.

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 10, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Tasdighi et al. (Tasdighi). Fig. 2 of Tasdighi shows a charge pump apparatus for generating output voltage supply Vout, wherein the apparatus comprises transfer capacitor C1; a plurality of transfer capacitor coupling switches SW1,SW2 with each switch effectively switchable between conducting and nonconducting states under control of a charge pump clock output from charge pump clock generating circuit 24. Coupling switches SW1 and SW2 can each comprise the CMOS inverter shown in Fig. 3 (e.g. see column 3, lines 37-43), wherein 26 and 27 can also be

considered a distinct transfer capacitor coupling switch. One of ordinary skill in the art would understand the operation of Tasdighi's circuit, which is also described on column 3, lines 16-36. Transfer capacitor C1 charges when switches SW1,SW2 couple the upper terminal of C1 to voltage source Vin and its lower terminal to Gnd; and discharges when the switches couple the upper terminal to Gnd and its lower terminal to output voltage supply Vout. Therefore, one of ordinary skill in the art would know the transfer capacitor is alternately charged and discharged in accordance with the clock output. The charging would occur during period first times, and the discharging would occur during periodic second times that are not concurrent with the first times. One of ordinary skill in the art would realize that charge pump clock generating circuit 24 would include circuitry that would inherently limit the rise rate of the clock output, as well as circuitry that would limit the fall rate of the clock output, thus anticipating claims 1-2. For example, to control the switches (e.g. 26 and 27 of Fig. 3), it is understood the clock output transitions between high and low levels. Whatever circuitry within generating circuit 24, which provides the clock output, would limit the rise and fall rates because the circuitry can handle only a maximum amount of current, which affects how fast the clock output can transition, thus limiting the transition rates. Also, it is noted that Tasdighi discloses the clock output can be changed by various ways (e.g. see column 4, lines 47-55). Therefore, one of ordinary skill in the art would interpret that as generating circuit 24 can include various types of circuitry that limits the rise/fall rates of the clock output. Since transfer capacitor C1 will be coupled to voltage source Vin in response to the charge pump clock output, the coupling can be considered via the charge pump clock output, and claim 10 is also anticipated. One of ordinary skill in the art would realize switches SW1 and SW2 of Tasdighi allow transfer capacitor C1 to be charged and

discharged in an alternative, non-overlapping, manner. Since a corresponding CMOS inverter of Fig. 3 can be used for each switch SW1,SW2, the apparatus of Tasdighi can be interpreted as comprising transfer capacitor C1; source switching device 26 can be disposed in series between transfer capacitor C1 and voltage source Vin; output switching device 27 can be disposed in series between transfer capacitor C1 and output voltage supply Vout; and charge pump clock generating circuit 24 is configured to provide a single-phase charge pump clock output coupled to the source switching device(s) and output switching device(s). Since it is understood the switches operate in a complementary manner, source switching device 26 of SW1 and device 26 of SW1 will conduct and allow transfer capacitor C1 to charge since the series current path is coupled between Vin and Gnd when the clock output is high, wherein output switching device 27 of SW2 and device 27 of SW1 will conduct and allow transfer capacitor C1 to discharge since the series current path will be coupled between Gnd and Vout when the clock output is low. [Note: The actual conduction and nonconduction periods, and the connections of the CMOS inverter in each switch SW1,SW2, will depend on if the charging operation is desired when the clock output is high, and the discharging operation is desired when the clock output is low. If the opposite operation was desired, PMOS 27 and NMOS 26 of the CMOS inverter would be reversed with respect to their connections to Vin, Gnd, and Vout.] These conducting/nonconducting operations anticipate claim 18.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In so far as being understood, claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tasdighi as applied to claim 18 above. Although Tasdighi's circuit and operation is understood to read on the limitations of claim 18, the reference does not show or disclose a second charge pump stage. However, it would have been obvious to one of ordinary skill in the art to add a second charge pump stage/apparatus to the charge pump apparatus of claim 18. It could have the same basic structure as Tasdighi's Fig. 2, wherein the second charge pump stage could be coupled in parallel to the charge pump apparatus, and both would receive the same charge pump clock output. Therefore, the second transfer capacitor C1 (of the stage) would be charged at the same time as C1 of the charge pump apparatus, and it would be discharged at the same time C1 of the charge pump apparatus is discharged. The first and second voltage sources would be Vin, and the first and second output voltage supplies would be Vout. Therefore, claim 19 is rendered obvious. Coupling two identically structured charge pump stages in parallel, both being controlled by the same clock output, would provide one known means for providing the output voltage supply Vout with twice the current a single stage would

provide. That extra current could be used if load 22 requires, or changes to require, more current than a single stage can provide.

Claims 3-9 (as applied to claim 1 above), claims 19-20 and 22 (as applied to claim 18 above), and claims 12, 14-17, 24-41, 43-51, 53-61, and 66-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tasdighi et al. (Tasdighi) in view of Hara et al. (Hara). As previously described above, Figs. 2/5 of Tasdighi shows/discloses a charge pump apparatus for generating an output voltage supply Vout, wherein the rise/fall rates are limited, and the periodic first/second times are understood. However, the reference does not clearly show or disclose current source/sink limit devices, circuitry configured to limit (source and/or sink) currents conducted by an amplifying driver circuit, or capacitive coupling circuit(s) to a coupling switch. However, Tasdighi does disclose the clock output of the oscillator can be changed by various ways (e.g. see column 4, lines 47-55), and the oscillator "could be a ring oscillator or any other known from of oscillator" (i.e. see column 5, lines 21-22). Fig. 13 of Hara shows the clock output of ring oscillator 89d being applied to the input of a charge pump type circuit 89e. Each of Figs. 1, 4-6, 8, and 10 of Hara show different embodiments of ring oscillators that can be used as ring oscillator 89d (i.e. see column 8, lines 59-61). These embodiments are disclosed with respect to current limiting (e.g. see column 3, lines 29-50), reducing power consumption (e.g. see column 3, lines 60-62), and changing the oscillation cycle (e.g. see column 2, lines 16-19 and 36-39). Therefore, it would have been obvious to one of ordinary skill in the art to use one of Hara's ring oscillators (e.g. Fig. 6) as the oscillator in Tasdighi's Fig. 2 apparatus. [Hara's Fig. 6 ring oscillator closely corresponds to the applicants' own Fig. 4 circuit, wherein the inverters 1a-5a,1d-5d of Hara are coupled to current mirror associated transistors 1b-6b to

provide limited source currents, and other current mirror associated transistors 1c-6c to provide limited sink currents.] Since current source limit device 5b limits the rise rate of clock output OUT, and current sink limit device 5c limits the fall rate of clock output OUT, claims 3 and4 are rendered obvious. With 1b-5b and 1c-5c limiting the currents conducted by their respective amplifying driver circuit (e.g. 5b,5c limit the currents of amplifying driver circuit 5a,5d), claims 7-8 are rendered obvious. The series connection of current mirror input transistors 6b and 6c allows substantially identical magnitudes of the limited source currents (via 1b-5b) and sink currents (via 1c-5c), rendering claim 9 obvious. Although neither reference clearly shows capacitive coupling circuit(s) to at least one transfer capacitor coupling switch, Fig. 20 of Hara shows capacitive coupling circuits (not labeled) connected to transistors 12p and 12n, which one of ordinary skill in the art would understand are types of coupling switches. Therefore, it would have been obvious to one of ordinary skill in the art to provide a respective capacitive coupling circuit between Hara's clock output OUT and the control node of each corresponding transfer capacitor coupling switch (e.g. SW1,SW2 or 26,27) of Tasdighi, thus rendering claims 5-6 obvious. The capacitive coupling circuits would provide one means for DC blocking to minimize possible transitioning errors. Interpreting Hara's Fig. 6 charge pump clock generating circuit in a different manner, the generating circuit includes an active driver circuit 5a,5d configured to source current (via 5a) to driver output node OUT, and sink current (via 5d) from the output node, wherein the generator circuit also includes circuitry 5b for limiting the source current, and circuitry 5c for limiting the current sunk. This interpretation renders obvious claim 12. Similar to claims 7-8, 5-6, and 9, claims 14, 15, and 17 are respectfully rendered obvious. Also, claim 16 is rendered obvious because Hara's oscillator circuit is one known type of a

current-starved ring oscillator. Circuitry 60,1b-5b,1c-5c of Hara's charge pump clock generating circuit limits currents conducted by each amplifying driver circuit (e.g. 1a/1d – 5a/5d), which one of ordinary skill in the art would understands will reduce the voltage change rates of clock output OUT during both positive and negative transitions. Therefore, claims 20 and 22 also rendered obvious. For the same reasoning as applied before with respect to the transfer capacitor, source switching device(s), output switching device(s), and the capacitive coupling circuit(s), claims 24-27 are rendered obvious. Interpreting the Tasdighi/ Hara circuitry as a method, a discharging TCS circuit (within switch SW2) of Tasdighi couples transfer capacitor (TC) to output supply Vout during discharge periods under control of first charge pump clock output OUT of Hara's ring oscillator (shown in Fig. 6); wherein 60,1b-5b1c-5c actively limit a rate of voltage change of clock output OUT during both positive and negative transitions, rendering claim 28 obvious. A charging TCCS circuit (with switch SW1) of Tasdighi couples transfer capacitor (TC) to source voltage Vin during charge periods under control of second charge pump clock output OUT of Hara's ring oscillator (shown in Fig. 6) that alternate nonoverlapplingly with the discharge periods (e.g. provide complementary charging and discharging); wherein 60,1b-5b1c-5c actively limit a rate of voltage change of second clock output OUT during both positive and negative transitions, rendering claim 29 obvious. First charge pump clock output OUT is the second charge pump clock output OUT, and claim 30 is rendered obvious. Since the first charge pump clock output OUT controls all the TCCS circuits (SW1,SW2 or 26,27) of Tasdighi, claim 31 is rendered obvious. By controlling when the switches become conductive or not conductive, the charge pump clock output effectively couples TC C1 to voltage source/source voltage Vin, rendering claim 32 obvious. Current limiting circuit

5b,5c limits the current drive capacity of charge pump clock output OUT, and claim 33 is rendered obvious. As previously described, first charge pump clock output OUT can be coupled to each TCS circuit by a corresponding capacitive coupling circuit, rendering obvious claims 34-35. First current limiting circuit 5b limits source currents from driver circuit 5a/5d, and second current limiting circuit 5c limits sink currents in driver circuit 5a,5d, and claim 36 is rendered obvious. Due to the current limiting relationships with respect to series connected 6b,6c, the source and sink currents have substantially identical magnitudes, and claim 37 is rendered obvious. First current limiting circuit 5b comprises a current mirror device 5b (e.g. with respect to 6b) and second current limiting circuit 5c comprises a different current mirror device 5c (e.g. with respect to 6c), rendering claim 38 obvious. 1b-5b and 1c-5c limit source and sink currents respectively to/from their corresponding driver circuits, and claim 39 is rendered obvious. Fig. 6 of Hara is one known type of current-starved ring oscillator, rendering claim 40 obvious. It would have been obvious to one of ordinary skill in the art to use a diode, or diode-connected transistor as a passive TCCS circuit to couple TC 31 to source voltage Vin or output supply Vout, rendering obvious claim 41. One of ordinary skill in the art understands a passive device (e.g. a diode) can be used in place of an active device (e.g. a transistor), when they are to be used as a switching device that is either conductive or nonconductive with respect to a clock output signal. Since claims 43-51, 53-61, and 66-67 are obvious variations of the limitations cited in the numerous claims already rejected within the previous descriptions, it is not considered necessary to keep repeating redundant type explanations. Therefore, claims 43-51, 53-61, and 66-67 are rendered obvious for the same reasoning as previously presented with respect to the other rejected claims.

Claims 3-9 (as applied to claim 1 above), claims 19-20 and 22-23 (as applied to claim 18) and claims 12-17, 24-41, 45-51, 53-61, and 66-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tasdighi et al. (Tasdighi) in view of Ito et al. (Ito). As previously described above, Figs. 2/5 of Tasdighi shows/discloses a charge pump apparatus for generating an output voltage supply Vout, wherein the rise/fall rates are limited, and the periodic first/second times are understood. However, the reference does not clearly show or disclose current source/sink limit devices, circuitry configured to limit (source and/or sink) currents conducted by an amplifying driver circuit/active driver circuits, capacitive coupling circuit(s) to a coupling switch, or a discrete capacitive element coupled to the driver output node. However, Tasdighi does disclose the clock output of the oscillator can be changed by various ways (e.g. see column 4, lines 47-55), and the oscillator "could be a ring oscillator or any other known from of oscillator" (i.e. see column 5, lines 21-22). Fig. 12 of Ito shows ring oscillator 70 providing clock output CLKO that can be controlled (via Vf, Vc, and the values of delay capacitors 51c-53c; see column 2, lines 5-47). Therefore, it would have been obvious to one of ordinary skill in the art to use Ito's ring oscillator 70 as the oscillator in Tasdighi's Fig. 2 apparatus. [Ito's Fig. 12 ring oscillator closely corresponds to the circuits shown in the applicants' own Figs. 4-5t, wherein the inverters 51a-53a,51b-53b of Ito are coupled to current mirror associated transistors 58-61 to provide limited source currents, and other current mirror associated transistors 62-64 to provide limited sink currents.] Since current source limit device 61 limits the rise rate of clock output CLKO, and current sink limit device 64 limits the fall rate of clock output CLKO, claims 3 and 4 are rendered obvious. With 58-61 and 62-64 limiting the currents conducted by their respective amplifying driver circuit (e.g. 61,64 limit the currents of amplifying driver circuit 53a,53b),

claims 7-8 are rendered obvious. The series connection of current mirror input transistors 58 and 57 allows substantially identical magnitudes of the limited source currents (via 59-61) and sink currents (via 62-64), rendering claim 9 obvious. It would have been obvious to one of ordinary skill in the art to provide a respective capacitive coupling circuit between Ito's clock output CLKO and the control node of each corresponding transfer capacitor coupling switch (e.g. SW1,SW2 or 26,27) of Tasdighi, thus rendering claims 5-6 obvious. The capacitive coupling circuits would provide one means for DC blocking to minimize possible transitioning errors. Interpreting Ito's Fig. 12 charge pump clock generating circuit in a different manner, the generating circuit includes an active driver circuit 53a/53b configured to source current (via 61) to driver output node CLKO and sink current (via 53b) from the output node, wherein the generator circuit also includes circuitry 61 for limiting the source current, and circuitry 64 for limiting the current sunk. This interpretation renders obvious claim 12. Discrete capacitive element 53c is coupled to driver output node CLKO, and its connection is understood to reduce voltage rates of change at the driver output node due to the known charging/discharging characteristics of a capacitor, rendering claim 13 obvious. 51a/51b, 52a/52b, and 53a/53b are each an active driver circuit configured to source and sink currents to their corresponding driver output node; circuitry 59-61 limits the current source capacity of each driver circuit; and circuitry 62-64 limits the current sink capacity of each driver circuit, and claim 14 is rendered obvious. As previously described above with respect to claims 5-6, capacitive coupling networks can be used to coupled clock output CLKO to the control node of active switches within the charge pump apparatus, thus claim 15 is rendered obvious. Due to the current limiting transistors 59-64, the ring oscillator of Ito is configured as one known type of a current-starved ring oscillator,

rendering obvious claim 16. The configuration of source current circuitry 58-61 and sink current circuitry 56, 62-64 will limit source and sink currents to substantially identical magnitudes, and claim 17 is rendered obvious. For the same reasoning as applied before with respect to prior art rejections described related to the Tasdighi/Hara references, and to prior art rejections described above with respect to claims 3-9, and 12-17 and the Tasdighi/Ito references, claims 19-20, 22-41, 43-51, 53-61, and 66-67 are also rendered obvious. These claims are obvious variations of the numerous claims already rejected within the previous descriptions, and it is not considered necessary to keep repeating redundant type explanations.

No claim is allowable as presently written.

Allowable Subject Matter

However, claims 11 and 21 are only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no motivation to modify or combine any prior art reference(s) to ensure: 1) the first and second control node AC impedances have the relationship (i.e. second AC impedance ≥ 2 * first impedance) as recited within claim 11; and 2) the first and second device areas have the relationship (i.e. second device area > 2 * first device area) as recited within claim 21.

Also, claims 26, 42, 52, and 62-65 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure: 1) the capacitive coupling circuit(s) also include biasing circuitry as recited within claim 26; 2) the control node AC

impedances have the relationship (i.e. discharge output TCCS AC impedance ≥ 2 * discharge common TCCS AC impedance) as recited within claim 42; 3) the control node AC impedances have the relationship (i.e. second discharging switch AC impedance ≥ 2 * first discharging switch AC impedance) as recited within claim 52; and 4) biasing each capacitive coupling network as recited within claim 62 (upon which claims 63-65 depend).

Prior Art

The other prior art reference cited on the accompanying PTO-892 is deemed relevant to at least sections of the claimed invention. Although not used in any formal rejections described above, Yokomizo et al. shows/discloses a transfer capacitor C1 that is alternately charged and discharged during complementary operations. These operations are performed in response to one clock output provided by oscillation circuit 13 (e.g. see Fig. 1). Since the operations are complementary, it would be understood by one of ordinary skill in the art that the unlabeled inverter could be removed from the circuit, if switches SW3-SW4 are replaced by their complementary switches. During operation, switches SW1-SW2 will be closed to allow C1 to charge while switches SW3-SW4 are opened. However, because of the complementary operation, when switches SW1-SW2 are opened, switches SW3-SW4 are closed to allow C1 to discharge to Vo. It is also noted that Fig. 3 of Yokomizo shows a charge pump apparatus comprising two transfer capacitors C1 and C3, along with their respective coupling switches.

The prior art references cited on the IDS submitted Feb 13, 2004 have been reviewed and considered. Dufour does not clearly show/disclose a transfer capacitance with the coupling switches. Although not used in any formal rejections, Fig. 3A of Nork et al. shows transfer capacitor 8 along with coupling switches S1-S4, that are controlled by complementary clock

signals VCLK,VCLKB, but one of ordinary skill in the art would know that the complementary charging and discharging operations of capacitor 8 could be made with respect to a single clock signal. Also, Fig. 9 of the Nork el al. reference shows a plurality of capacitors. Butler also shows a transfer capacitor and corresponding coupling switches. However, these switches are controlled by three clock signals. The Lascari reference does not show any circuits, and therefore, the transfer capacitor and associated coupling switches are not clearly disclosed. Although the LTC1550L/LTC1551L reference does disclose charge pump related descriptions, it shows no circuit, and therefore the transfer capacitor and coupling switches are not clearly disclosed. Design Note 243 shows a charge pump type apparatus with a capacitor in Fig. 3, and discloses the input current of both phases of the charge pump clock are regulated, but does not clearly show or disclose the coupling switches and/or current limiting devices as recited within the present application's claims. The second page of the TI reference clearly shows two separate charge pump type apparatus, each with a transfer capacitor and four corresponding coupling switches. Similar to the Nork et al. reference, the switches with the TI apparatus are apparently controlled by complementary signals, which one of ordinary skill in the art would understand could be replaced by a single clock signal, as long as the complementary charging and discharging type operations still occur. The Maxim reference also shows two separate charge pump type apparatus, each with its own transfer capacitor and coupling switches. Although these switches are apparently controlled by a single output SWITCH CONTROL, this reference was also not cited in any of the formal rejections described above, which used references that provided additional circuitry and/or operational descriptions.

Between these various prior art references cited above, and the knowledge of one of ordinary skill in the arts, the current limiting within a ring oscillator; the alternate charging and discharging of a transfer (e.g. flying or pump) capacitor; and the use of a (ring) oscillator to control a charge pump apparatus, are all well known and understood by one of ordinary skill in the art. Therefore, these limitations are not considered as describing a novel circuit or method. Most of these references should be carefully reviewed and considered with respect to the broadest reasonable interpretations of the cited claim limitations.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

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